REMARKS

Applicants respectfully traverse and request reconsideration.

Applicants again wish to thank the Examiner for notice that claims 29-31 would be allowable if written in independent form. However as noted below, Applicants respectfully note that the references may have been misapprehended and as such, the other claims are also in condition for allowance.

Claims 1, 4-9, 19, 22-23 and 25-27 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi and Venkat. As a preliminary matter, Applicants respectfully withdraw the previous statement that claim 1 includes forming a configurable register. However, Applicants also respectfully note that the "Response to Arguments" section does not address any of Applicants' arguments with respect to Gillespie, Surugucchi or Venkat provided in the previous response. Accordingly Applicants respectfully reassert the relevant remarks and if the claims are not allowed, Applicants respectfully request a non-final action that addresses Applicants remarks.

The Examiner suggests that it would be obvious to one of ordinary skill in the art to combine the teachings of Gillespie and Surugucchi et al. to render the data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs in order to consolidate configuration. However, Surugucchi et al. explicitly teach that the BASS control logic unit updates the registers in the second configuration register space (which includes the BASS 1 memory mask) with the values in the first configuration space when the values in the first configuration space are set and/or modified. (See column 8, lines 47-51.) Therefore, Surugucchi et al. explicitly teach away from using a read only memory for storing mask values because the BASS control logic would not be able to update a read only memory. Accordingly,

it would not be obvious for one skilled in the art to combine the teachings of Gillespie and Surugucchi et al. to render the data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs in order to consolidate configuration.

Venkat fails to cure the deficient teachings of Gillespie and Surugucchi et al. As best understood by Applicants, Venkat discloses a bus interface device for interfacing a secondary peripheral bus with a system having a host CPU and a primary peripheral bus. The bus interface of Venkat enables "virtual integration" of multiple physically distinct peripheral devices so that the collection of devices can function as a single integrated unit. The "virtually integrated" devices can share resources such as a dedicated bus, memory space, and memory bandwidth just as if the devices were physically integrated. An intelligent device configuration process and a dynamic internal memory map allow each peripheral device to be independently added to the system, removed from the system, or upgraded just as if each device was a completely separate peripheral. The bus interface provides a dedicated secondary bus that enables multimedia and graphics bus traffic to be isolated from the CPU's primary peripheral bus. Applicants can find no mention of data bridge having a read only memory for storing mask values for each ASIC of the plurality of ASICs. Therefore, reconsideration and withdrawal of the rejection of claim 1 is respectfully requested.

As such, Applicants respectfully submit that the claims are in condition for allowance.

Claims 2-3, 20-21, 24 and 33 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi and Venkat as applied to claim 1 and further in view of Applicants' admitted prior art. Applicants respectfully reassert the relevant remarks made above and as such, these claims are also in condition for allowance.

Claim 28 stands rejected under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 6,675,292 (Prabhu). Applicants respectfully submit that it appears that the Prabhu reference has been misapprehended. In particular, column 5, lines 40-56 of Prabhu has been cited as teaching a circuit having a configurable register that includes register configuration logic and at least one register flop that contains an initial value and at least one mask flop that generates a mask bit for the configuration logic and wherein the register configuration logic configures the at least one register flop to be read and/or writable based upon the at least one mask value. (See page 5 of rejection). However, Prabhu is directed to an exception handling operation for SIMD floating point instruction using a floating point status register to report exceptions. The cited paragraph actually refers to a preconfigured register block that as known in the art may have different types of registers namely general purpose registers, status registers and control registers. Some of the general purpose registers are only visible to an integer execution unit and some are only visible to graphics unit. In addition, the status registers and control registers, as known in the art, contain condition and control codes relating to the processor's operation. The last sentence of the paragraph states "although some status and control registers can be modified by program instructions, [so that they can be written to or read from] many registers may be configured as read only." (Column 5, lines 54-56). The use of the word "configured" in this context refers to the fact that status and control registers may be preconfigured at manufacture to be both read and write registers but some may be read only registers. There is no register configuration logic described because there is no configurable register. The office action alleges that the claimed configuration logic is apparently inherent. Applicants respectfully submit that it is not inherent and respectfully challenge this assertion since the reference does not teach any logic in a circuit that configures configurable registers to read and/or write registers as claimed.

Prabhu describes a preconfigured register block. In addition, there are no mask flops that generate a mask bit for any configuration logic in Prabhu as alleged and there is no part of Prabhu that has been cited for teaching such structure. This is likely because Prabhu does not teach the claimed subject matter.

The claim requires that the configuration logic configures the register flop to be read and/or writable based on at least one mask value stored in the memory. The cited portion of Prabhu again does not provide for any configuration logic that configures the register flop to be writable as opposed to readable based on at least one mask value stored in the memory but instead refers to standard circuits that simply have register blocks wherein some of those registers are fabricated as read only registers and others are fabricated to be read and writable when they are manufactured. Accordingly, the claims are allowable for one or more of these reasons.

In addition, official notice is taken that configuration memory as claimed is well known. If the claim is not passed to allowance, Applicants respectfully challenge the official notice and request specific documentation showing the teaching of a circuit that includes memory containing initial values and mask values for use in forming a register as claimed. In addition, Applicants respectfully submit that for argument sake, even if such a configuration memory is known, combining such memory with that of Prabhu would not result in the claimed invention since Prabhu uses preformed registers some of which may be read only even though they are status or control registers as described by Prabhu. Accordingly, Applicants respectfully submit that the claim is in condition for allowance.

Claims 10-11, 13, 15-17 and 34-35 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi and Venkat as applied to claim 1 and further

in view of Prabhu. Applicants respectfully reassert the remarks made above with respect to Prabhu as Prabhu does not teach configurable registers as alleged but to the contrary refers to configured registers that may be read only.

The dependent claims add additional novel and non-obvious subject matter.

Claims 14 and 18 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Gillespie in view of Surugucchi, Venkat and Prabhu as applied to claim 10 and further in view of Applicants' admitted prior art. Applicants respectfully reassert the relevant remarks made above with respect to the Prabhu reference and as such, these claims are also in condition for allowance. Applicants also respectfully note that if the claims are not allowed, Applicants respectfully request a showing by column and line number of where the references teach the claimed subject matter of claims 14 and 18 since these claims require, for example, initial values and mask values stored in the read only memory that define configuration registers in the data bridge as a function of the configuration requirements of the graphics processor. This language is not addressed in the rejection.

The other dependent claims are allowable for at least depending upon an allowable base claim.

Applicants respectfully submit that the claims are in condition for allowance and respectfully request that a timely Notice of Allowance be issued in this case. The Examiner is invited to contact the below-listed attorney if the Examiner believes that a telephone conference will advance the prosecution of this application.

Respectfully submitted,

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